

WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:
a plurality of nonvolatile memory cells each
having a gate, a drain and a source to hold data
5 corresponding to a threshold voltage level;
a plurality of word lines connected to gates of
the nonvolatile memory cells, respectively;
a plurality of bit lines connected to drains of
the nonvolatile memory cells, respectively;
10 a plurality of source lines connected to sources
of the nonvolatile memory cells, respectively;
a reference current generation circuit which
generates a reference current, the reference current
generation circuit including at least one reference
15 cell and an amplification circuit which amplifies
a current flowing through the reference cell, and
a ratio of an amplification factor of current in
a program verify mode to an amplification factor of
current in a data read mode is larger than 1; and
20 a sense amplifier which compares the reference
current with a current flowing through selected ones of
the nonvolatile memory cells and reads data held in the
selected ones of the nonvolatile memory cells.
2. The nonvolatile semiconductor memory according
25 to claim 1, wherein a gate voltage of said at least one
reference cell is equal to a voltage that is applied to
word lines connected to the selected ones of the

nonvolatile memory cells in the data read mode.

3. The nonvolatile semiconductor memory according to claim 1, wherein a verify voltage in the program verify mode is equal to a voltage that is applied to word lines connected to the selected ones of the nonvolatile memory cells in the data read mode.

4. A nonvolatile semiconductor memory comprising:
a plurality of nonvolatile memory cells each having a gate, a drain and a source to hold a multilevel of three or more levels corresponding to a threshold voltage level;

a plurality of word lines connected to gates of the nonvolatile memory cells, respectively;

a plurality of bit lines connected to drains of the nonvolatile memory cells, respectively;

a plurality of source lines connected to sources of the nonvolatile memory cells, respectively;

a reference current generation circuit which generates at least first and second reference currents, the reference current generation circuit including at least a first reference cell, a second reference cell having a threshold voltage that is higher than that of the first reference cell, a first amplification circuit which amplifies a current flowing through the first reference cell, and a second amplification circuit which amplifies a current flowing through the second reference cell, a first current amplification ratio of

an amplification factor of current in program verify mode to an amplification factor of current in a data read mode in the first amplification circuit being larger than 1, a second current amplification ratio of an amplification factor of current in a program verify mode to an amplification factor of current in a data read mode in the second amplification circuit being larger than 1, and the first current amplification ratio being smaller than the second current amplification ratio;

a first sense amplifier which compares the first reference current with a current flowing through a selected one of the nonvolatile memory cells and reads a signal corresponding to a multilevel held in the selected one of the nonvolatile memory cells; and

a second sense amplifier which compares the second reference current with a current flowing through a selected one of the nonvolatile memory cells and reads a signal corresponding to a multilevel held in the selected one of the nonvolatile memory cells.

5. The nonvolatile semiconductor memory according to claim 4, wherein a gate voltage of each of the first and second reference cells is equal to a voltage that is applied to word lines connected to the selected one of the nonvolatile memory cells in the data read mode.

6. The nonvolatile semiconductor memory according to claim 4, wherein a voltage applied to word lines

connected to the selected one of the nonvolatile memory cells in the program verify mode is equal to a voltage that is applied to word lines connected to the selected one of the nonvolatile memory cells in the data read mode.

7. The nonvolatile semiconductor memory according to claim 4, wherein the reference current generation circuit further includes a third reference cell having a threshold voltage which is higher than that of the second reference cell in order to generate a third reference current, and a third amplification circuit which amplifies a current flowing through the third reference cell.

8. The nonvolatile semiconductor memory according to claim 7, wherein:

the first amplification circuit includes the first reference cell, and the first reference current (I_{ref0}) in the data read mode is generated by $a0 \times I_{refcell0}$ and the first reference current (I_{ref0}) in the program verify mode is generated by $b0 \times I_{refcell0}$ when a ratio of first transconductance of a first current non-converting p-type MOS transistor to second transconductance of a first read current converting p-type MOS transistor is 1 : $a0$, a ratio of the first transconductance of the first current non-converting p-type MOS transistor to third transconductance of a first verify current converting p-type MOS transistor

is $1 : b_0$, and a threshold voltage of the first reference cell is V_{t0} and a cell current at a time of application of gate voltage (V_r) is $I_{refcell0}$;

the second amplification circuit includes the
5 second reference cell, and the second reference current (I_{ref1}) in the data read mode is generated by $a_1 \times I_{refcell0}$ and the second reference current (I_{ref1}) in the program verify mode is generated by $b_1 \times I_{refcell1}$ when a ratio of fourth transconductance of a second
10 current non-converting p-type MOS transistor to fifth transconductance of a second read current converting p-type MOS transistor is $1 : a_1$, a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to sixth transconductance of
15 a second verify current converting p-type MOS transistor is $1 : b_1$, and a threshold voltage of the second reference cell is V_{t1} ($V_{t1} > V_{t0}$) and a cell current at a time of application of gate voltage (V_r) is $I_{refcell1}$; and

20 the third amplification circuit includes the third reference cell, and the third reference current (I_{ref2}) in the data read mode is generated by $a_2 \times I_{refcell2}$ and the third reference current (I_{ref2}) in the program verify mode is generated by $b_2 \times I_{refcell2}$ when a
25 ratio of seventh transconductance of a third current non-converting p-type MOS transistor to eighth transconductance of a third read current converting

p-type MOS transistor is $1 : a_2$, a ratio of the seventh transconductance of the third current non-converting p-type MOS transistor to ninth transconductance of a third verify current converting p-type MOS transistor is $1 : b_2$, and a threshold voltage of the third reference cell is V_{t2} ($V_{t2} > V_{t1} > V_{t0}$) and a cell current at a time of application of gate voltage (V_r) is $I_{refcell2}$.

9. The nonvolatile semiconductor memory according to claim 7, further comprising a third sense amplifier which compares the third reference current with a current flowing through the bit lines from the non-volatile memory cells and reads a signal corresponding to a multilevel held in each of the nonvolatile memory cells.

10. The nonvolatile semiconductor memory according to claim 4, wherein the reference current generation circuit further includes a third amplification circuit which amplifies a current flowing through the second reference cell in order to generate a third reference current.

11. The nonvolatile semiconductor memory according to claim 10, wherein:

the first amplification circuit includes the first reference cell, and the first reference current (I_{ref0}) in the data read mode is generated by $a_0 \times I_{refcell0}$ and the first reference current (I_{ref0}) in the program

verify mode is generated by $b_0 \times I_{refcell0}$ when
a ratio of first transconductance of a first current
non-converting p-type MOS transistor to second
transconductance of a first read current converting
5 p-type MOS transistor is $1 : a_0$, a ratio of the first
transconductance of the first current non-converting
p-type MOS transistor to third transconductance of
a first verify current converting p-type MOS transistor
is $1 : b_0$, and a threshold voltage of the first
10 reference cell is V_{t0} and a cell current at a time of
application of gate voltage (V_r) is $I_{refcell0}$;

the second amplification circuit includes the
second reference cell, and the second reference current
(I_{ref1}) in the data read mode is generated by $a_1 \times$
15 $I_{refcell0}$ and the second reference current (I_{ref1}) in
the program verify mode is generated by $b_1 \times I_{refcell1}$
when a ratio of fourth transconductance of a second
current non-converting p-type MOS transistor to fifth
transconductance of a second read current converting
20 p-type MOS transistor is $1 : a_1$, a ratio of the fourth
transconductance of the second current non-converting
p-type MOS transistor to sixth transconductance of
a second verify current converting p-type MOS
transistor is $1 : b_1$, and a threshold voltage of the
25 second reference cell is V_{t1} ($V_{t1} > V_{t0}$) and a cell
current at a time of application of gate voltage (V_r)
is $I_{refcell1}$; and

the third amplification circuit includes the second reference cell, and the third reference current (I_{ref2}) in the data read mode is generated by $a2 \times I_{refcell1}$ and the third reference current (I_{ref2}) in the program verify mode is generated by $b2 \times I_{refcell1}$ when a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to seventh transconductance of a third read current converting p-type MOS transistor is $1 : a2$, a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to eighth transconductance of a third verify current converting p-type MOS transistor is $1 : b2$, and a threshold voltage of the second reference cell is V_{t1} and a cell current at a time of application of gate voltage (V_r) is $I_{refcell1}$.

12. The nonvolatile semiconductor memory according to claim 10, further comprising a third sense amplifier which compares the third reference current with a current flowing through a selected one of the non-volatile memory cells and reads a signal corresponding to a multilevel held in the selected one of the nonvolatile memory cells.

13. A nonvolatile semiconductor memory comprising:
a plurality of nonvolatile memory cells each having a gate, a drain and a source to hold a multilevel of three or more levels corresponding to

a threshold voltage level;

a plurality of word lines connected to gates of the nonvolatile memory cells, respectively;

5 a plurality of bit lines connected to drains of the nonvolatile memory cells, respectively;

a plurality of source lines connected to sources of the nonvolatile memory cells, respectively;

10 a reference current generation circuit which selectively generates at least first and second reference currents, the reference current generation circuit including at least a first reference cell, a second reference cell having a threshold voltage that is higher than that of the first reference cell, a first amplification circuit which amplifies a current
15 flowing through the first reference cell, and a second amplification circuit which amplifies a current flowing through the second reference cell, a first current amplification ratio of an amplification factor of current in program verify mode to an amplification factor of current in a data read mode in the first
20 amplification circuit is larger than 1, a second current amplification ratio of an amplification factor of current in a program verify mode to an amplification factor of current in a data read mode in the second
25 amplification circuit is larger than 1, and the first current amplification ratio is smaller than the second current amplification ratio; and

a sense amplifier which compares an output
current of the reference current generation circuit and
a cell current flowing through a selected one of the
nonvolatile memory cells and amplifies and outputs the
5 cell current.

14. The nonvolatile semiconductor memory according
to claim 13, wherein the reference current generation
circuit further includes a third reference cell having
a threshold voltage which is higher than that of the
10 second reference cell in order to generate a third
reference current, and a third amplification circuit
which amplifies a current flowing through the third
reference cell.

15. The nonvolatile semiconductor memory according
15 to claim 14, wherein:

the first amplification circuit includes the first
reference cell, and the first reference current. (I_{ref0})
in the data read mode is generated by $a0 \times I_{refcell0}$
and the first reference current (I_{ref0}) in the program
20 verify mode is generated by $b0 \times I_{refcell0}$ when
a ratio of first transconductance of a first current
non-converting p-type MOS transistor to second
transconductance of a first read current converting
p-type MOS transistor is 1 : $a0$, a ratio of the first
25 transconductance of the first current non-converting
p-type MOS transistor to third transconductance of
a first verify current converting p-type MOS transistor

is $1 : b_0$, and a threshold voltage of the first reference cell is V_{t0} and a cell current at a time of application of gate voltage (V_r) is $I_{refcell0}$;

the second amplification circuit includes the
5 second reference cell, and the second reference current (I_{ref1}) in the data read mode is generated by $a_1 \times I_{refcell0}$ and the second reference current (I_{ref1}) in the program verify mode is generated by $b_1 \times I_{refcell1}$ when a ratio of fourth transconductance of a second
10 current non-converting p-type MOS transistor to fifth transconductance of a second read current converting p-type MOS transistor is $1 : a_1$, a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to sixth transconductance of
15 a second verify current converting p-type MOS transistor is $1 : b_1$, and a threshold voltage of the second reference cell is V_{t1} ($V_{t1} > V_{t0}$) and a cell current at a time of application of gate voltage (V_r) is $I_{refcell1}$; and

20 the third amplification circuit includes the third reference cell, and the third reference current (I_{ref2}) in the data read mode is generated by $a_2 \times I_{refcell2}$ and the third reference current (I_{ref2}) in the program verify mode is generated by $b_2 \times I_{refcell2}$ when a
25 ratio of seventh transconductance of a third current non-converting p-type MOS transistor to eighth transconductance of a third read current converting

p-type MOS transistor is $1 : a_2$, a ratio of the seventh transconductance of the third current non-converting p-type MOS transistor to ninth transconductance of a third verify current converting p-type MOS transistor is $1 : b_2$, and a threshold voltage of the third reference cell is V_{t2} ($V_{t2} > V_{t1} > V_{t0}$) and a cell current at a time of application of gate voltage (V_r) is $I_{refcell2}$.

16. The nonvolatile semiconductor memory according to claim 14, further comprising a third sense amplifier which compares the third reference current with a current flowing through the bit lines from the non-volatile memory cells and reads a signal corresponding to a multilevel held in each of the nonvolatile memory cells.

17. The nonvolatile semiconductor memory according to claim 13, wherein the reference current generation circuit further includes a third amplification circuit which amplifies a current flowing through the second reference cell in order to generate a third reference current.

18. The nonvolatile semiconductor memory according to claim 17, wherein:

the first amplification circuit includes the first reference cell, and the first reference current (I_{ref0}) in the data read mode is generated by $a_0 \times I_{refcell0}$ and the first reference current (I_{ref0}) in the program

verify mode is generated by $b_0 \times I_{refcell0}$ when
a ratio of first transconductance of a first current
non-converting p-type MOS transistor to second
transconductance of a first read current converting
5 p-type MOS transistor is $1 : a_0$, a ratio of the first
transconductance of the first current non-converting
p-type MOS transistor to third transconductance of a
first verify current converting p-type MOS transistor
is $1 : b_0$, and a threshold voltage of the first
10 reference cell is V_{t0} and a cell current at a time of
application of gate voltage (V_r) is $I_{refcell0}$;
the second amplification circuit includes the
second reference cell, and the second reference current
(I_{ref1}) in the data read mode is generated by $a_1 \times$
15 $I_{refcell0}$ and the second reference current (I_{ref1}) in
the program verify mode is generated by $b_1 \times I_{refcell1}$
when a ratio of fourth transconductance of a second
current non-converting p-type MOS transistor to fifth
transconductance of a second read current converting
20 p-type MOS transistor is $1 : a_1$, a ratio of the fourth
transconductance of the second current non-converting
p-type MOS transistor to sixth transconductance of a
second verify current converting p-type MOS transistor
is $1 : b_1$, and a threshold voltage of the second
25 reference cell is V_{t1} ($V_{t1} > V_{t0}$) and a cell current
at a time of application of gate voltage (V_r) is
 $I_{refcell1}$; and

the third amplification circuit includes the second reference cell, and the third reference current (I_{ref2}) in the data read mode is generated by $a2 \times I_{refcell1}$ and the third reference current (I_{ref2}) in the program verify mode is generated by $b2 \times I_{refcell1}$ when a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to seventh transconductance of a third read current converting p-type MOS transistor is 1 : $a2$, a ratio of the fourth transconductance of the second current non-converting p-type MOS transistor to eighth transconductance of a third verify current converting p-type MOS transistor is 1 : $b2$, and a threshold voltage of the second reference cell is V_{t1} and a cell current at a time of application of gate voltage (V_r) is $I_{refcell1}$.

19. A nonvolatile semiconductor memory comprising:
a plurality of nonvolatile memory cells each having a gate, a drain and a source to hold a multilevel of three or more levels corresponding to a threshold voltage level;

a plurality of word lines connected to gates of the nonvolatile memory cells, respectively;

a plurality of bit lines connected to drains of the nonvolatile memory cells, respectively;

a plurality of source lines connected to sources of the nonvolatile memory cells, respectively;

a reference current generation circuit which selectively generates at least first and second reference currents, the reference current generation circuit including at least a first reference cell,
5 a second reference cell having a threshold voltage that is higher than that of the first reference cell, a first amplification circuit which amplifies a current flowing through the first reference cell, and a second amplification circuit which amplifies a current flowing
10 through the second reference cell, a first current amplification ratio of an amplification factor of current in program verify mode to an amplification factor of current in a data read mode in the first amplification circuit being larger than 1, a second
15 current amplification ratio of an amplification factor of current in a program verify mode to an amplification factor of current in a data read mode in the second amplification circuit being larger than 1, and the first current amplification ratio is smaller than the
20 second current amplification ratio, the reference current generation circuit further including a third reference cell having a threshold voltage which is higher than that of the second reference cell in order to generate a third reference current, and a third
25 amplification circuit which amplifies a current flowing through the third reference cell; and
a sense amplifier which compares an output

current of the reference current generation circuit and a cell current flowing through a selected one of the nonvolatile memory cells and amplifies and outputs the cell current,

5 wherein the reference current generation circuit selectively outputs the second and third reference currents in accordance with logic of an output of the sense amplifier when the output current of the reference current generation circuit is the first
10 reference current.

20. A nonvolatile semiconductor memory comprising:
a plurality of memory cells each having 2^N (N is two or more) levels;

a plurality of word lines connected to gates of
15 the memory cells, respectively;

a plurality of bit lines connected to drains of the memory cells, respectively;

a plurality of source lines connected to sources of the memory cells, respectively;

20 a reference current generation circuit which selectively outputs one of (N-1) reference currents, the reference current generation circuit including (N-1) reference cells and (N-1) amplification circuits which amplify a current flowing through the (N-1)
25 reference cells, a threshold voltage of a first reference cell of the (N-1) reference cells being higher than that of a (I-1)-th reference cell ($1 \leq I \leq$

N), a ratio of an I-th amplification factor of current in program verify mode to an amplification factor of current in a data read mode in an I-th amplification circuit of the (N-1) amplification circuits being
5 larger than 1, and a (I-1)-th amplification factor being smaller than the I-th amplification factor; and

a sense amplifier which compares an output current of the reference current generation circuit and a cell current flowing through a selected one of the memory
10 cells and amplifies and outputs the cell current,

wherein the reference current generation circuit selectively outputs the second and third reference currents in accordance with logic of an output of the sense amplifier when the output current of the
15 reference current generation circuit is the first reference current.

21. A nonvolatile semiconductor memory comprising:

a plurality of memory cells each having 2^N (N is two or more) levels;

20 a plurality of word lines connected to gates of the memory cells, respectively;

a plurality of bit lines connected to drains of the memory cells, respectively;

25 a plurality of source lines connected to sources of the memory cells, respectively;

a reference current generation circuit which selectively outputs one of (N-1) reference currents,

the reference current generation circuit including
(N-1) reference cells and (N-1) amplification circuits
which amplify a current flowing through the (N-1)
reference cells, a threshold voltage of a first
5 reference cell of the (N-1) reference cells being
higher than that of a (I-1)-th reference cell ($1 \leq I \leq$
N), a ratio of an I-th amplification factor of current
in program verify mode to an amplification factor of
current in a data read mode in an I-th amplification
10 circuit of the (N-1) amplification circuits being
larger than 1, and a (I-1)-th amplification factor
being smaller than the I-th amplification factor; and
a sense amplifier which compares an output current
of the reference current generation circuit and a cell
15 current flowing through a selected one of the memory
cells and amplifies and outputs the cell current,
wherein the reference current generation circuit
selectively outputs the second and third reference
currents in accordance with logic of an output of the
20 sense amplifier when the output current of the
reference current generation circuit is the first
reference current.